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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,245	12/17/2001	Scott T. Becker	ARTCP012C	8144

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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,245	BECKER, SCOTT T.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 have been presented for examination based on applicant's disclosure filed on 17 December 2001. Claims 1-11 have been rejected by the examiner.

Drawings

2. The drawing Figure 3B is objected to because the sectional portion of the drawing is not referenced to Figure 3D. Correction is required.

Priority

3. Applicant's claim for domestic priority as a continuation of Application No. 09/422,877 (now US 6,470,304) filed 18 November 1999 is acknowledged.

Specification

4. The disclosure is objected to because of the following informalities:

The "means for" language recited on page 7 lines 7-10 of the specification is improper and does not provide the necessary enablement for the claimed subject matter. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. *The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.*

Specifically, independent claims 1 and 11 include limitations relating to the memory core having a "depth that is defined by a plurality of words" and "a word width that is defined by multiple pairs" of bitlines but no specific description of how the depth is defined by the word, or how a word width is defined by multiple pairs of bitlines is given. While page 6, lines 10, 21, and page 7, line 7 of the specification make reference to "a memory core having a depth that defines a plurality of words, and a word width that is defined by multiple pairs" (of bitlines), there is no specific definition or format given that describes the relationship between the claimed word and the memory core "depth", or the claimed word width and the multiple pairs of bitlines. Figures 1-3D do not cure this deficiency. Further, the "means for" language recited on page 7 lines 7-10 of the specification is improper and does not provide the necessary enablement for the claimed subject matter. (see objection to the specification above) Accordingly, a skilled artisan would not know how to make and/or use the claimed invention from the description contained in the specification.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 12-22 of U.S. Patent No. 6,016,390.

Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 12-22 of U.S. 6,016,390 are drawn to the same limitations as claims 1-11 of the present invention. These include:

- *memory core having depth defined by words*
- *word width defined by pairs (global/complementary) of bitlines*
- *designing core cell - global/complementary bitlines*
- *designing flipped core cell with global/complementary bitlines*
- *arranging core cell followed by flipped core cell*

For example, independent claim 12 of U.S. 6,016,390 recites an identical preamble to claim 1 of the present invention and nearly identical limitations with

the only exception being the recitation of a six transistor core cell instead of simply a core cell. This is obvious from a motivational standpoint since the specification for the present invention discloses only six transistor memory core cells including global bitlines. (See Figure 3A) Dependent claims 2-11 similarly include functionally equivalent features relating to flipped complementary bitlines, pairs of flipped core cells, cross-coupled inverters (P-type, N-type), and multi-layer interconnect structure.

The examiner therefor asserts that these limitations are obvious in of U.S. 6,016,390 independent claim 12 since they are functionally equivalent in operation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-14 are rejected under 35 U.S.C. 103 as being unpatentable over US Patent 5,999,482 issued to Kornachuk et al in view of US Patent 6,043,562 issued to Keeth.

Independent claims 1 and 12 are drawn to memory device with reduced bitline capacitance by:

- *memory core having depth defined by words*
- *word width defined by pairs (global/complementary) of bitlines*
- *core cell with global/complementary bitlines*
- *flipped core cell with global/complementary bitlines*

- *core cells alternating by core cell and flipped core*

Per independent claims 1 and 12: Kornachuk discloses the elements of the claimed limitations of the present invention as follows:

- a memory core having depth defined by words: Kornachuk teaches a memory core design having a model wordline defining the memory core configuration. (Abstract, Summary of Invention, CL4-L1-23, 40-64, Figs. 2-3) Since the specification for the present invention gives no formal definition for the claimed word and word width limitations (see 112(1) rejection), the examiner has equated the model wordline of Kornachuk to be functionally equivalent to the word and word width definitions of the present invention.

*- word width defined by pairs (global/complementary) of bitlines: Kornachuck discloses **globally** addressable core cells (CL4-L14-23, CL7-L4, Fig. 7) and complementary bitlines (CL5-L39, Fig. 3) and defining a model wordline of the memory core configuration (CL4-L1-23, 40-64, Figs. 2-3).*

*- a core cell with global/complementary bitlines: Kornachuk discloses **globally** addressable core cells (CL4-L14-23, CL7-L4, Fig. 7) and complementary bitlines (CL5-L39, Fig. 3).*

*- flipped core cell with global/complementary bitlines: Kornachuk discloses **globally** addressable core cells (CL4-L14-23, CL7-L4, Fig. 7) and complementary bitlines (CL5-L39, Fig. 3) connected to inverted (flipped) transistor core. (Figs. 3-5)*

Kornacheu does not explicitly teach that core cells alternate (folded array) with a flipped core.

Keeth discloses a semiconductor memory technique with multiple layers and offset conductive levels with cross coupled transistor pairs in the reduction of physical size. (abstract, Fig. 7, 30, 31,33, Detailed Description CL4-L55, CL5-L3) Keeth also discloses a memory core design having a model wordline defining the memory core configuration (Figs. 9-19, Tables 1-11) and a core cell followed by flipped (complementary) core cell pair. (Abstract, Summary of Invention, CL2-L15, CL4-L35-55, CL7-L29-31, Figs. 7, 9-19) Most importantly, Keech teaches an alternating folded array architecture and using digitline pairs in the core cell. (CL21-L41-45, CL22-L37-43, Fig. 39)

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Kornachuk relating to memory core design having a model wordline defining the memory core configuration and complementary bitlines, with the teachings of Keeth relating to core cells alternating (folded array architecture) with a flipped core, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many types of memory core cell designs available in the market place and large amounts of money being spent in product development and improvement. (see Keeth Background, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence,

would have been motivated to modify the teachings of Kornachuk with the teachings of Keeth in order to reduce development time and cost.

Regarding dependent claims 2-10: In addition to the limitations already addressed above, dependent claims include additional limitations which are disclosed in the prior art (Keeth) as follows:

- *cross-coupled P-type and N-Type transistors: (Keeth discloses cross-coupled P-type and N-Type transistors: CL5-L3-5, Fig. 9)*
- *four transistor cell on multi-layer polysilicon: (Keeth discloses a four transistor cell on multi-layer polysilicon: CL10-L52-53, Fig. 22)*

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,288,969 issued to Gibbins et al teaches high-speed asynchronous memory with current sensing amplifiers.

U.S. Patent 5,748,547 issued to Shau teaches high performance embedded semiconductor memory devices with multiple dimension first level bit lines.

U.S. Patent 5,179,538 issued to Pang et al teaches six transistor core cell memory with current sensing amplifiers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-

305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.

Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900. The Official Fax Numbers are:

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August 12, 2004

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